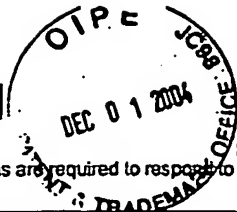


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		Application Number	10/720,672
		Filing Date	November 25, 2003
		First Named Inventor	NOVAKOVSKY, Alexander
		Group Art Unit	2183 2825
		Examiner Name	Not yet known TUYEN TO
		Attorney Docket Number	P-5667-US
Sheet	1	of	1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (where appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
TT	A	Jolly, Simon; Parashkevov, Atanas; McDougall, Tim: "Automated Equivalence Checking of Switch Level Circuits", pgs. 299-304; DAC 2002, June 10-14, 2002, New Orleans, Louisiana, USA.	<input type="checkbox"/>
TT	B	Kuehlmann, A.; Srinivasan, A.: "Verity - a formal verification program for custom CMOS circuits": IBM Journal of Research & Development, Jan-Mar 95, Vol. 39, Issue 1 of 2, p. 149, 17p., 3 charts, 9 diagrams	<input type="checkbox"/>
TT	C	Fischer et al. "Abstraction of Schematic to High Level HDL Design", Technology, Intel Israel (74) Ltd. ICCAD 1990, pp. 90-96	<input type="checkbox"/>
TT	D	Kam et al., "Comparing Layouts with HDL Models: A Formal Verification Technique", IEEE, 1992, pp. 588-591	<input type="checkbox"/>
TT	E	Kam et al., "State Machine Abstraction from Circuit Layouts using BDD's: Application in Verifications and Synthesis", IEEE, 1992, pp. 92-97	<input type="checkbox"/>
TT	F	Lester et al.: LIP6/ASIM Laboratory, University Pierre et Marie Curie-Paris: "Yagle, a second generation functional abstractor for CMOS VLSI Circuits", 1998, pp. 265-268	<input type="checkbox"/>
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TT	H	Bryant, "Extraction of gate level models from transistor circuits by four valued symbolic analysis", IEEE, 1991, pp. 350-353	<input type="checkbox"/>
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Examiner Signature <i>Tuyen To</i>	Date Considered 10/20/2005
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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609 Draw line through citation if not in conformance and not considered Include copy of this form with next communication to applicant

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